

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Accompanying Continuation Application under 37 CFR  
1.53(b) :

Prior Application: Y. OKAMOTO et al  
USSN 09/567,158  
Filed: May 9, 2000

Group Art Unit: 1756  
Examiner: N. BARRECA  
For: PROCESS FOR FABRICATING SEMICONDUCTOR  
INTEGRATED CIRCUIT DEVICE, AND  
EXPOSING SYSTEM AND MASK INSPECTING  
METHOD TO BE USED IN THE PROCESS

JC979 U.S. PTO  
09/922656  
08/07/01

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents  
Washington, D.C. 20231

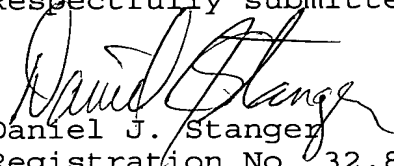
August 7, 2001

Sir:

In accordance with the duty of disclosure, the applicants  
inform the Examiner of the documents cited during prosecution  
of the parent application, USSN 09/567,158.

The applicants request the Examiner to initial and return  
a copy of the attached PTO-1449 form as an indication that the  
references have been considered.

Respectfully submitted,

  
Daniel J. Stanger  
Registration No. 32,846  
Attorney for Applicant(s)

MATTINGLY, STANGER & MALUR  
1800 Diagonal Rd., Suite 370  
Alexandria, Virginia 22314  
(703) 684-1120  
Date: August 7, 2001